REMARKS

Claims 1-18 are currently pending in the Application. Claim 17 is currently amended to clarify the subject matter of the claimed invention, without acquiescence in the cited basis for rejection or prejudice to pursue the original claim in a related application. No new matter has been added.

I. Allowable Subject Matter

Applicants would like to thank the Examiner for finding claims 1-2, 8, and 13-16 to be allowable over the prior art of record.

Applicants would further like to thank the Examiner for providing detailed explanation for the basis for each objection and rejection.

II. Rejections of the Claims under 35 U.S.C. § 112, First Paragraph

Claims 5-7 and 9-12 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicants respectfully traverse.

Applicants respectfully point to several examples in the Specification which provide clear written description to enable one of ordinary skill in the art to make and use the claimed invention. Applicants further respectfully note that the following examples are provided for illustration and explanation purposes only and do not intend to limit the scope of the claimed invention as embodied in these claims.

Applicants first respectfully point to *p. 3, l. 20-p. 4, l. 6* which provides, as some background information and to the extent pertinent, that "[t]he value 'Z', however, does not represent a state of either 0 or 1. The value 'Z' . . . represents the state of a signal not being driven or floating . . . When not actively driving a signal, an electronic device, such as a logic gate or other digital circuit, may present a high-impedance state, or 'Z' state, at its output. . . ."

Applicants then respectfully point to *p. 13, ll. 10-16* which illustrate some embodiments of the claimed invention. These passages show that when an analog circuit block receives a Z value (i.e., floating value) of an input (i.e., the input is not being driven), simulator 100 enables the analog circuit block to **solve for that node as if it were an output of the analog block**. *P. 19, l. 18-p. 20,*

l. 7 further illustrates that, in some embodiments, when input to analog block 203 is a Z value, then such an input to analog circuit block 203 is not being driven by another device or circuit (). In this case, simulator 100 solves for the analog circuit block 203 absent the input to analog block 203 and propagates the analog block solution (i.e., signal value) to other fanouts of net 202 **using the output portion of the analog ioput**. These passages clearly provide sufficient written description to enable one of ordinary skill in the art to make and use the claimed invention as encompassed in claim 5 which, in part, recites "simulating the circuit design by modeling at least one of said output . . . **as an analog output signal** from said analog circuit to said node when said at least one of said output is **in said high impedance state**" (emphasis added.)

In addition, Applicants respectfully point to p. 12, l. 16-p. 13, l. 9 which states, to the extent pertinent, "when digital gate 201 drives any non-Z value onto network node 202, every fanout of net 202 including analog circuit block 203 connected to net 202 (analog block 203 in this example includes, among other things, components R1/R2 and transistor devices M1/M2) receive this non-Z value as an input. However, when digital gate 201 is not driving an output signal of 0, 1, or X, digital gate 201 presents a Z value (i.e., floating) output onto net 202 . . . ." That is, when the digital gate 201 drives any non-Z value (i.e., not floating or not in high impedence state), every fanout of net 202 including analog circuit block 203 receives this non-Z value as an input rather than output as illustrated in the preceding paragraph immediately above when the digital circuit block is not driving any non-Z values. Applicants therefore respectfully submit that these exemplary paragraphs clearly provide sufficient written description for the claimed invention of the independent claim 5 which recites, to the extent pertinent, "simulating the circuit design by modeling at least one of said output **as a digital output signal** from the corresponding digital circuit to said node when said at least one of said output is **not in said high impedance state** . . ." (emphasis added.)

Therefore, Applicants respectfully submit that since claim 9 recites similar limitations as does claim 5, and claims 6-7 and 10-12 depend from claims 5 and 9 respectively, claim 5-7 and 9-12 are believed to have satisfied the requirements under 35 U.S.C. § 112, first paragraph. Applicants thus respectfully request the withdrawal of the rejections and reconsideration of these claims.

III. Rejections of the Claims under 35 U.S.C. § 112, Second Paragraph

Claims 3-4 and 17-18 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. More specifically, the Office Action provides that "[t]he limitation appears to assign both a high impedance state value and an analog signal value to the output when the output is in a high impedance state." Applicants respectfully disagree.

A. For claim 3:

Claim 3 recites, to the extent pertinent, "simulating the circuit design by modeling said output **as a digital output signal from said digital circuit** to said node when said output is **not in said high impedance state**, and **as an analog output signal from said analog circuit** to said node **when said output is in said high impedance state**" (emphasis added.) That is, the above limitation explicitly states that when the output is in a high impedance state, the method models the output as an analog output signal from the analog circuit to the node, and that when the output is not in the high impedance state, the method models the output as a digital output signal from the digital circuit to the node. That is, depending upon whether the output is in a impedance state, the method models the output as an analog output signal from the analog circuit or as a digital output signal from the digital circuit.

As such, claim 3 does not assign both a high impedance state value and an analog signal value to the output as alleged by the Office Action. Applicants thus respectfully request withdrawal of the rejections and reconsideration of these claims.

B. For claim 17:

Applicants respectfully submit that claim 17 is currently amended and is believed to have overcome the rejection under 35 U.S.C. § 112, second paragraph. Applicants thus respectfully request withdrawal of the rejection and reconsideration of claim 17.

CONCLUSION

Based on the foregoing, it is believed that, with entry of this amendment, all claims are now allowable and a Notice of Allowance is respectfully requested. If the Examiner has any questions or comments regarding this amendment, the Examiner is respectfully requested to contact the undersigned.

Applicant(s) hereby explicitly retracts and rescinds any and all of the arguments and disclaimers presented to distinguish the prior art of record during the prosecution of all parent and related application(s)/patent(s), and respectfully requests that the Examiner re-visit the prior art that such arguments and disclaimers were made to avoid.

The Commissioner is authorized to charge any fees due in connection with the filing of this document to Bingham McCutchen's Deposit Account No. **50-4047**, referencing billing number **7010652001**. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Bingham McCutchen's Deposit Account No. **50-4047**, referencing billing number **7010652001**.

Respectfully submitted,

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